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[SPLIT GATE FLASH MEMORY CELL AND MANUFACTURING METHOD THEREOF]

Abstract

A split gate flash memory cell includes a substrate having a device isolation structure; a selective gate structure disposed on the substrate; an interlayer dielectric layer having an opening disposed on the substrate, wherein the opening exposes a portion of the selective gate structure, the substrate and the device isolation structure; a floating gate disposed in the opening and extended to cover a surface of the interlayer dielectric layer; a tunneling dielectric layer disposed between the floating gate and the selective gate structure; a gate dielectric layer disposed between the floating gate and the control gate; a source region disposed in the substrate on one side of the control gate that is not adjacent to the selective gate structure, and a drain region disposed in the substrate on one side of the selective gate that is not adjacent to the control gate.